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Study of Switching Circuit for Parallel Computing

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ABSTRACT

Parallel computing and switching circuits have become a crucial topic in the concern of computer science and also it is revealed to be critical when researching high performance. This Study helps the process of breaking down larger processes into smaller and independent tasks, which helps to perform operations with various properties such as atomicity, consistency; isolation, and switching features. They also help manage faults in architecture, the results of which are combined upon completion as part of an overall algorithm. In this paper firstly we convert the graphical model of the perfect difference network into a circuit diagram then convert the circuit diagram into a switching function, then simplify it and redraw the equivalent network.

1 Introduction

The last few decades have witnessed an upsurge of parallel computing. Unprecedented growth in the research work being published in the related field. Since 2000 there have been many group work consistently. Now around 23 years over 1000 research papers or books are available. The switching devices used in digital systems are generally two-state devices, so it is natural to use binary numbers in system logic, and other building blocks are used to design circuits and logical operations elaborate on how to interconnect the building block to connect the input to the desired output. This paper elaborates on the relationship between input and output with the mathematical model using polynomial expression. This paper is concerned with parallel computing for solving large problems in a parallel environment.

2 Perfect Difference Network

Perfect Difference Network architecture, based on a PDS is designed where each i^{th} node is connected via direct links to nodes $i \pm 1$ and $i \pm s_j$ (mod n), for $2 \le j \le \delta$. Each link is bidirectional and the preceding connectivity leads to a chordal ring of δ in-degree and δ out-degree (total degree of a node $d(v) = 2\delta$) and diameter $D = 2$[1][2][3]. PDN has already been studied for, high-performance communication and parallel processing network [4] and some topological properties of PDNs and parallel algorithms [5][6][7][8] were suggested. It was shown that an n-node PDN can emulate the complete network with optimal slowdown and balanced message traffic. Although other interconnection architectures with topological and performance characteristics similar to PDNs exist, we view PDNs as worthy additions to the repertoire of computer system designers. The existence of perfect difference sets seems intuitively improbable, at any rate for large δ, but in 1938 J. Singer proved that, whenever δ is a prime or power of prime, say $\delta = p^n$, a perfect difference set mod $p^{2n} + p^n + 1$ exists. [1][8] [9][10].

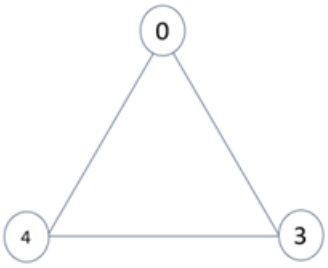
From now on, let δ denote p^n and we write that $n = \delta^2 + \delta + 1 = p^{2n} + p^n + 1$. $S = \{s: |s_i - s_j|$ *mod* n, where $0 \le i, j \le \delta$, $i \ne j$, δ is a prime or power of prime and $n = \delta^2 + \delta + 1\}$.

2.1 Circuit Analysis:

Perfect Difference network (PDN) has a galaxy of circuits, some of them shown below:

S.No	Closed Circuits	Size
Starting at node 0 (0-0), the circuits found are.		
1	0 → 4 → 3 → 0	3
2	0 → 4 → 1 → 0	3
3	0 → 3 → 6 → 0	3
4	0 → 6 → 5 → 1 → 0	4
5	0 → 6 → 5 → 4 → 0	4
6	0 → 1 → 2 → 6 → 0	4
7	0 → 1 → 2 → 3 → 0	4
8	0 → 1 → 2 → 3 → 6 → 0	5
9	0 → 1 → 2 → 3 → 4 → 0	5
10	0 → 6 → 5 → 2 → 1 → 0	5
11	0 → 6 → 5 → 4 → 1 → 0	5
12	0 → 6 → 5 → 4 → 3 → 0	5
13	0 → 6 → 5 → 4 → 3 → 2 → 1→ 0	7
Starting at node 1 (1-0), the circuits found are.		
14	1 → 5 → 4 → 1	3
15	1 → 5 → 2 → 1	3
16	1 → 4 → 3 → 2 → 1	4
17	1 → 5 → 4 → 3 → 2 → 1	5
Starting at node 2 (3-1), the circuits found are.		
18	2 → 6 → 5 → 2	3
19	2 → 3 → 6 → 2	3
20	2 → 5 → 4 → 3 → 2	4
21	2 → 6 → 5 → 4 → 3 → 2	5
Starting at node 3 (3-0), the circuits found are.		
22	3 → 6 → 5 → 4 → 3	4

From the above study, it is proved that the perfect difference network is the superset of balanced trees, therefore, one threaded spanning tree will be considered as a circuit of minimum size



0-3-4-0

(number of nodes in circuit) which is 3 and maximum path length is ($\delta^2 + \delta + 1$) which is chordal ring also an odd no. Here we consider a circuit starting with node 0 with minimum size:

Above figure is a one of circuit, used within PDN. There are 3 nodes combinations of these nodes with finite application of the binary operations and the unary operations are represent as function in Boolean nature. The nature of PDN circuit is Boolean nature, so we get value 1 or 0 as input and output. the logic [11][12] of above circuit is represented as 3 nodes function, have 2^3=8 and possible combinations are [13]:

2.2 Light Day Engine

N0(Light)	N3(Sunlight)	N4(Eng)	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	11	1	1

2^n Powerset of n element circuit having Boolean nature has 2^n element. These elements are in canonical form as represented as $2^3 = 8$.

$$\boldsymbol{N_0N_3N_4} + \boldsymbol{N_0N_3}N_4+\boldsymbol{N_0}N_3\boldsymbol{N_4} + \boldsymbol{N_0}N_3N_4+N_0\boldsymbol{N_3N_4} +N_0\boldsymbol{N_3}N_4+ N_0N_3\boldsymbol{N_4}+N_0N_3N_4$$

converting polynomial into Boolean matrix. Each node has a distinct function, but N_0 represents current/ Light, N_3→ Sunlight, N_4→ Engine/ Motor Now, convert the above logic into an expression

$$Y(N_0, N_3, N_4) = \Sigma_m(1, 4, 6, 7)$$

Then sum of the monomial function is considered a polynomial expression.

3 Conclusion

In this paper, we elaborate on one circuit of perfect difference networks. This investigation provides useful communication patterns in the design of new fault-tolerant, high-speed switching networks. Efforts have been made to find the involvement of links and nodes within the circuits of perfect difference networks. The robustness of architecture has been seen by calculating the node involvement in the circuits within the Perfect Difference Network.

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